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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,139	07/09/2003	Jung-Chien Chang	39524.0069	8097

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EXAMINER	
LIN, JAMES	
ART UNIT	**PAPER NUMBER**
1762	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/615,139	CHANG, JUNG-CHIEN	
	Examiner	Art Unit	
	Jimmy Lin	1762	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/5/2006 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 4 and 17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support for forming a conductive layer on the second circuit layer into the microvias to connect the first and second circuit layers (claim 4). The specification only provides support for forming a second circuit layer into the microvias to connect to the first circuit layer (see, e.g., pg. 6, lines 3-7).

There is no support for forming a gap to expose a portion of the resin layer between two sections of the second circuit layer when more than two circuit layers are deposited (claim 17). For the purpose of this examination, the claim will be interpreted to forming a gap in the topmost circuit layer.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 5-8, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikegami et al. (U.S. Publication 2003/0160339) in view of Kurita et al. (U.S. Patent 6,399,891) and Murakami (U.S. Publication 2002/0068382).

Ikegami teaches a method of making an electronic component (abstract), wherein a first circuit layer 7 is formed on a substrate 15. An electronic element 9 is electrically connected to the first circuit layer, an encapsulant layer 11 is applied, and the substrate is removed ([0031], [0037] – [0038]; Figs. 2A – 8).

Ikegami does not explicitly teach depositing a resin-copper coating on the first circuit layer and connecting electronic components to the topmost circuit layer. However, Ikegami does teach connecting an electronic element connected to the first circuit layer. Kurita teaches a method of making an electronic element that has connecting parts that are subjected to low thermal stress and is free from breakage at connecting parts (cols. 1-3), wherein the electronic element comprises a resin layer 16 and a copper layer 26 (abstract; Fig. 1). Electronic components 110, such as transistors, can be connected to the topmost circuit layer (col. 1, lines 13-19; Fig. 3b). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have electrically connected the electronic element of Kurita onto the first circuit layer of Ikegami so as to take advantage of an electronic element having low thermal stress at the connecting parts.

Ikegami and Kurita do not explicitly teach that the substrate is removed after the step of connecting the electronic components to the topmost circuit layer. However, Ikegami does teach that the encapsulant layer is applied before removing the substrate. Therefore, the electronic

component of Kurita must necessarily be connected to the topmost circuit layer before applying the encapsulant layer and removing the substrate.

Ikegami and Kurita do not explicitly teach that a second circuit layer is formed such that a gap is formed between two sections of the second circuit layer to expose a portion of the resin layer. However, Murakami teaches that electrical connection points on a circuit board can be made from a multilayer structure of gold deposited onto nickel deposited onto copper. In other words, gold is the top-most layer with copper being the bottom layer and nickel being the middle layer. Kurita teaches that electronic components can be connected to the top-most electrical copper layer (col. 1, lines 13-19; Fig. 3b). The selection of something based on its known suitability for its intended use has been held to support a prima facie case of obviousness. Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have used a copper/nickel/gold layer structure in forming the top-most electrical layer 26 of Kurita with a reasonable expectation of success because Murakami teaches that such a conductive structure is operable when forming connection points on a circuit board. Thus, the gold layer is interpreted to be the second circuit layer. As taught by Kurita, portions of the resin layer 16 are exposed to form the pattern of layer 26 (Fig. 1) and an electronic component is connected to the multiple sections on the second circuit layer (Fig. 2a). The electronic component covers at least part of the resin layer.

Claim 2: Ikegami teaches that the substrate has a plurality of fine holes and electrically conductive protrusions are formed on portions of the conductive film ([0013], [0033]; Fig. 4). By definition, a hole can be an indentation or depression. A dimple is also defined as a slight indentation or depression in a surface.

Claim 3: Ikegami teaches that the substrate has a flat surface between the holes (Fig. 4).

Claims 5-8: The electronic component is disposed on the exposed portion of the resin layer within the gap, as discussed above. Ikegami, Kurita, and Murakami do not explicitly teach that the electronic component is bonded to the second circuit layer with bonding wires. However, Ikegami does teach that bonding wires are suitable to electrically connect two components [0031]. The selection of something based on its known suitability for its intended use has been held to support a prima facie case of obviousness. Sinclair & Carroll Co. v.

Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have used bonding wires to have connected the electronic component to the second circuit layer because Ikegami teaches that such electrical connections are operable in the art.

Claim 17: Kurita teaches that a second circuit layer 22 and a third circuit layer 23 can be deposited before forming the topmost circuit layer 26 (Fig. 1).

Claims 18-19: Kurita does not explicitly teach that the electronic component is disposed within the gap. However, whether the conductive bumps 112 (Fig. 2a) sits squarely on the topmost circuit layer pattern 26 or is placed off center such that the center of the conductive bumps hang over the edge of the topmost circuit layer pattern (which could happen if the electronic component 110 is not aligned properly onto board 1), the electronic component would function properly. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have placed the conductive bumps off center as opposed to placing it squarely with a reasonable expectation of success because one of ordinary skill in the art would have recognized that both electrical connections are operable equivalents. Thus, the electronic component is at least partially disposed within the gap.

In addition, the electronic component is embedded in the gap of Kurita and in the encapsulant of Ikegami.

Claim 20: The electronic component is disposed across the gap.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikegami '339 in view of Kurita '891 and Murakami '382 as applied to claim 1 above, and further in view of Yamazaki et al. (U.S. Publication 2002/0079503).

Ikegami, Kurita, and Murakami are discussed above. Kurita teaches that holes are formed in the resin layers and between the conductive layers and filled with electrically conductive material by plating or other means to electrically connect the various layers (column 5, lines 43 – 51), but does not teach that a conductive layer is formed on the second circuit layer into the vias. However, Yamazaki teaches a conductive layer 262 can be formed over a circuit layer 257 and into a via to electrically connect two different regions (Fig. 5C). The selection of something based on its known suitability for its intended use has been held to support a prima

facie case of obviousness. Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have formed a conductive layer on the second circuit layer into the vias of Kurita to connect different circuit layers with a reasonable expectation of success because Kurita is open to various means for forming the electrical connection and because Yamazaki teaches that such a layer for connecting two electrical regions is operable in the art of electrical devices.

7. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikegami '339 in view of Kurita '891 and Murakami '382 as applied to claims 1-4 above, and further in view Farnworth (US 6,365,501).

Ikegami, Kurita, and Murakami are discussed above. Kurita teaches that the electronic component can be disposed across the gap (Fig. 2a-b). Kurita also teaches that the electronic component can be connected with solder balls 112 (col. 1, lines 13-19), but does not teach that the solder balls are made of tin. However, Farnworth teaches that solder balls are generally formed of lead and tin and are used to join a chip to a carrier such as printed wiring board (column 3, lines 5 – 21). The selection of something based on its known suitability for its intended use has been held to support a prima facie case of obviousness. Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have used tin solder balls as the particular solder material with a reasonable expectation of success because Farnworth teaches that such materials are suitable for making solder balls.

8. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikegami '339 in view of Kurita '891 and Murakami '382 as applied to claims 1-4 above, and further in view of Lin et al. (US 5,200,362), Carey et al. (US 5,672,260), and Meyrat et al. (US 4,842, 536).

Ikegami, Kurita, and Murakami are discussed above, but do not explicitly teach that multiple isolating layers are applied to adjacent sections of the exposed first circuit layer after the

substrate is removed. However, Lin teaches a method of fabricating a semiconductor device, wherein the substrate is removed and isolating layers 23 can be applied to the exposed surface of the pattern of conductive traces 13 (column 3, line 66 – column 4, line 1; Fig. 6). Openings 24 are formed through the isolating films to expose selected portions of the pattern of conductive traces (column 4, lines 3 – 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have applied an isolating layer to the exposed first circuit layer of Ikegami. One would have been motivated to do so in order to expose only selected portions of the traces and to protect the non-selected portions.

Ikegami, Kurita, Murakami, and Lin do not explicitly teach applying tin paste to the first circuit layer between adjacent isolating layers. However, Ikegami does teach that the exposed first circuit layer can be surface-mounted on an external printed wiring substrate through electrically conductive adhesive. Meyrat teaches that a tin paste soldering material can be arranged on a circuit board, wherein surface mounted devices are then connected with the tin. Printed circuits manufactured this way can accommodate more components per unit surface area (col. 1, lines 12-33). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to apply tin paste to the selected portions of the exposed pattern of conductive traces of Lin. One would have been motivated to do so with the expectation of connecting the conductive traces to surface mounted devices in a space efficient manner.

Response to Arguments

9. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Lin whose telephone number is 571-272-8902. The examiner can normally be reached on Monday thru Friday 8AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Meeks can be reached on 571-272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JL

JL

KEITH HENDRICKS
PRIMARY EXAMINER